I Claim:

1. A memory circuit, comprising:

a memory cell array including a plurality of memory cells, a plurality of word lines, and a plurality of bit lines, said plurality of memory cells being addressable via said plurality of word lines and bit lines;

a plurality of primary sense amplifiers for reading out, via said plurality of bit lines, data from said plurality of memory cells in accordance with a read-out address;

a plurality of secondary sense amplifiers, each of said plurality of secondary sense amplifiers including a latch;

a plurality of switching devices, a group of said plurality of primary sense amplifiers being connected to an assigned one of said plurality of said secondary sense amplifiers via a group of said plurality of switching devices for applying a datum from one of said plurality of primary sense amplifiers of said group to said assigned one of said plurality of secondary sense amplifiers via one of said plurality of switching devices selected by a read-out address; and

a test control unit configured for reading out data by connecting some of said plurality of switching devices in

parallel depending on a test mode signal and depending on the read-out address, so that in each case, one of said group of primary sense amplifiers is connected to said assigned one of said plurality of secondary sense amplifiers.

2. The memory circuit according to claim 1, further comprising:

a data bus;

said plurality of secondary sense amplifiers being individually connected to said data bus in accordance with a read-out signal for successively reading out data via said data bus.

3. The memory circuit according to claim 1, wherein each of said plurality of secondary sense amplifiers has an activation input for accepting data from a respective one of said plurality of primary sense amplifiers in accordance with an activation signal.

4. The memory circuit according to claim 1, further comprising:

an address decoder for selecting at least one of said plurality of said switching devices in accordance with an address;

said address decoder connected to at least one of said plurality of switching devices.

5. The memory circuit according to claim 4, wherein:

said address decoder has an input for obtaining the test mode signal; and

depending on the test mode signal, only a part of an address, which is applied to said address decoder, is taken into account for selecting one of said plurality of switching devices.

6. The memory circuit according to claim 5, wherein:

the address, which is applied to said address decoder, includes more significant address bits and less significant address bits; and

the part of the address, which is applied to said address decoder, that is taken into account corresponds to the less significant address bits.

7. A method for reading out data from a memory circuit while testing the memory circuit, which comprises:

providing a memory cell array including a plurality of memory cells, a plurality of word lines, and a plurality of bit lines, the plurality of memory cells being addressable via the plurality of word lines and bit lines;

using a plurality of primary sense amplifiers to read out, via the plurality of bit lines, data from the plurality of memory cells in accordance with a read-out address;

assigning each one of a plurality of secondary sense amplifiers to a respective group of the plurality of primary sense amplifiers;

switchably connecting a group of the plurality of primary sense amplifiers to an assigned one of the plurality of the secondary sense amplifiers to apply a datum from one of the plurality of primary sense amplifiers to the assigned one of the plurality of secondary sense amplifiers; and

depending on a test mode signal and depending on the read-out address, simultaneously applying data to a secondary sense

amplifier from a respective primary sense amplifier of the group of the plurality of primary sense amplifiers.

8. The method according to claim 7, which further comprises successively reading out the data from the plurality of secondary sense amplifiers.